**In the Specification**

*Please revise the paragraph beginning on page 18, line 1 as follows:*

In the present invention, the deep trench capacitor may be provided within the deep trenches 18 by known techniques including, for example, the technique of Rupp, et al., *Extending Trench DRAM Technology to 0.15μm Groundrule and Beyond,* IEDM Proceedings, page 33-36, 1999~~, herein incorporated by reference~~. In forming the deep trench capacitor, the trenches 18 may be provided with a deep trench capacitor comprising a buried plate diffused electrically around the exterior of the deep trenches. As illustrated in the cross sectional view along dashed line 101 of Fig. 7, Fig. 9 illustrates that the deep trench capacitor may be provided within the deep trenches 18 by providing the buried plate comprising an isolation collar 220 diffused electrically around the exterior of the deep trenches. The isolation collar 220 may be provided directly under the self-aligned shallow trench isolation structure comprising the merged thermal silicon dioxide regions 30, thereby making direct contact with the silicon dioxide regions 30 and filling any gaps therebetween. Furthermore, the isolation collar 220 is provided in the upper, external regions of the trench 18 lying there-under the merged thermal silicon dioxide regions 30 by known techniques. The isolation collar 220 may comprise a material as known and used in the art including silicon dioxide, silicon nitride, and the like, and may be provided in such upper, external regions of the trench 18 to a thickness of about 3 nm to about 50 nm. In the

preferred embodiment, the isolation collar 220 comprises silicon dioxide provided to a thickness of about 30 nm.

*Please revise the paragraph beginning on page 19, line 6 as follows:*

Subsequently, the vertical transistor may be provided on the sidewalls within each of the deep trenches 18 by techniques as known and used in the art such as, for example, those techniques as disclosed in Gruening, et al., *A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd Strap (VERI BEST) for 4Gb/16Gb,* IEDM Proceedings, page 25-28, 1999; and Radens, et al., *A 0.135 $\mu m^2$ $6F^2$ Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM,* IEDM Proceedings, page 80-81, 2000~~, herein incorporated by reference~~.